

ABSTRACT OF THE DISCLOSURE

A video codec (1) is provided in which a frame sync (FS) in base-band video data is delayed a predetermined time. A processor (14) is provided to make interrupt in a timing that is based on the delayed frame sync and make settings for input/output processing with respect to input/output modules (11 and 13). The processor (14) makes interrupt in a timing which is based on any of the delayed frame sync, video clock (V. Clk) and system clock (Sys. Clk) to control encoding or decoding start timing of a codec module (12). Thus, base-band video data can be encoded and decoded in a steady input/output timing.